

A cross-sectional view of a semiconductor device. The device features a central channel region (3) flanked by source (S) and drain (D) regions. The channel region contains a series of gates (34a, 34b) and a central gate (35). The source and drain regions are doped with N+ and P- ions. The device is surrounded by a protective layer (1) and a substrate (2). The gates are labeled 31, 32, 33, 34a, 34b, and 35. The source and drain regions are labeled S and D. The channel region is labeled 3. The protective layer is labeled 1. The substrate is labeled 2. The gates are labeled 31, 32, 33, 34a, 34b, and 35. The source and drain regions are labeled S and D. The channel region is labeled 3. The protective layer is labeled 1. The substrate is labeled 2.

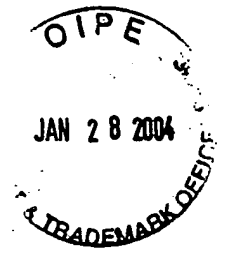


FIG. 33

